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AMENDMENTS TO CLAIMS

- Please cancel claims 2, 12, and 17.
- Please amend claims 1, 6-11, and 16.
- Please add new claims 21-24.

A complete listing of all claims and their status in the application are as follows:

1. (currently amended) A method of forming an integrated circuit comprising:
providing a semiconductor substrate;
forming a gate dielectric on the semiconductor substrate;
forming a gate on the gate dielectric;
forming an insulating sidewall spacer around the gate;
forming source/drain junctions in the semiconductor substrate;
forming a silicide on the source/drain junctions and on the gate;
forming trenches in the semiconductor substrate around the gate at the outer edge of
the insulating sidewall spacer;
forming an interlayer dielectric above the semiconductor substrate; and
forming contacts in the interlayer dielectric to the silicide.
2. (cancelled)
3. (original) The method as claimed in claim 1 wherein:
forming the trenches uses an etching process that etches the semiconductor substrate.
4. (original) The method as claimed in claim 1 wherein:
forming the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.
5. (original) The method as claimed in claim 1 wherein:
forming the contacts to the silicide uses materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.
6. (currently amended) A method of forming an integrated circuit comprising:
providing a semiconductor substrate;

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forming a gate dielectric on the semiconductor substrate;
forming a gate on the gate dielectric;
forming source/drain junctions in the semiconductor substrate;
forming a silicide on the source/drain junctions and on the gate
~~forming a sidewall an insulating~~ spacer around the gate;
forming trenches in the semiconductor substrate at the outer edges of the insulating
sidewall spacer;
forming an interlayer dielectric above the semiconductor substrate; and
forming contacts in the interlayer dielectric to the silicide.

7. (currently amended) The method as claimed in ~~claim 1~~ claim 6 wherein
forming the sidewall spacer further comprises:

forming an insulating liner around the gate; and
forming an insulating film having a cusp over the insulating liner; and
removing the insulating film and the insulating liner at the cusp.

8. (currently amended) The method as claimed in ~~claim 1~~ claim 6 wherein:
forming the trenches uses an etching process that etches the semiconductor substrate

9. (currently amended) The method as claimed in ~~claim 1~~ claim 6 wherein:
forming the interlayer dielectric deposits a dielectric material having a dielectric
constant selected from a group consisting of medium, low, and ultra-low
dielectric constants.

10. (currently amended) The method as claimed in ~~claim 1~~ claim 6 wherein:
forming the contacts to the ~~ultra-uniform~~ silicide uses materials selected from a group
consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy
thereof, a compound thereof, and a combination thereof.

11. (currently amended) An integrated circuit comprising:
a semiconductor substrate;
a gate dielectric on the semiconductor substrate;
a gate on the gate dielectric;
an insulating spacer around the gate;
source/drain junctions in the semiconductor substrate;

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a silicide on the source/drain junctions and on the gate;
trenches in the source/drain junctions of the semiconductor substrate around the gate
outer edge of the insulating spacer;
an interlayer dielectric above the semiconductor substrate; and
contacts in the interlayer dielectric to the silicide.

12. (cancelled)

13. (original) The integrated circuit as claimed in claim 11 wherein:
the trenches extend into the semiconductor substrate to a level lower than the silicide.

14. (original) The integrated circuit as claimed in claim 11 wherein:
the interlayer dielectric comprises a dielectric material having a dielectric constant
selected from a group consisting of medium, low, and ultra-low dielectric
constants.

15. (original) The integrated circuit as claimed in claim 11 wherein:
the contacts to the silicide comprises materials selected from a group consisting of
tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound
thereof, and a combination thereof.

16. (currently amended) An integrated circuit comprising:
a semiconductor substrate;
a gate dielectric on the semiconductor substrate;
a gate on the gate dielectric;
source/drain junctions in the semiconductor substrate;
a silicide on the source/drain junctions and on the gate;
~~a sidewall spacer around the gate;~~
an insulating liner around the gate;
an insulating film over the insulating liner;
trenches in the semiconductor substrate at the outer edges of the ~~sidewall spacer~~
insulating film;
an interlayer dielectric above the semiconductor substrate; and
contacts in the interlayer dielectric to the silicide.

17. (cancelled)

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18. (original) The integrated circuit as claimed in claim 16 wherein:
the trenches extend into the semiconductor substrate to a level lower than the silicide.
19. (original) The integrated circuit as claimed in claim 16 wherein:
the interlayer dielectric deposits a dielectric material having a dielectric constant
selected from a group consisting of medium, low, and ultra-low dielectric
constants.
20. (original) The integrated circuit as claimed in claim 16 wherein:
the contacts to the silicide comprise materials selected from a group consisting of
tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound
thereof, and a combination thereof.
21. (new) A method of forming an integrated circuit comprising:
providing a semiconductor substrate;
forming a gate dielectric on the semiconductor substrate;
forming a gate on the gate dielectric;
forming a sidewall spacer around the gate;
forming a cusp at the outer edge of the sidewall spacer;
removing the sidewall spacer at the cusp;
forming source/drain junctions in the semiconductor substrate;
forming a silicide on the source/drain junctions and on the gate;
forming trenches in the semiconductor substrate at the outer edge of the sidewall
spacer;
forming an interlayer dielectric above the semiconductor substrate; and
forming contacts in the interlayer dielectric to the silicide.
22. (new) The method as claimed in claim 21 wherein:
forming the trenches uses an etching process that etches the semiconductor substrate.
23. (new) The method as claimed in claim 21 wherein:
forming the interlayer dielectric deposits a dielectric material having a dielectric
constant selected from a group consisting of medium, low, and ultra-low
dielectric constants.

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24. (new) The method as claimed in claim 21 wherein:
forming the contacts to the silicide uses materials selected from a group consisting of
tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound
thereof, and a combination thereof.